

Serial SCSI Host Storage Interface Core DATASHEET

Overview

IntelliProp's IPR-SS100C is an industry standard Serial-SCSI (SAS) host interface core that enables host application companies to use high throughput SAS storage devices. The protocol interface is compliant to the SAS 2.04 specification as defined by the International Committee for Information Technology Standards. The IPR-SS100C is fully verified in pseudo random simulation.

Applications

The IPR-SS100C is available for integration into host ASIC and FPGA designs to provide an industry compliant SAS 3.0 Gb/s interface for host designs. Some of the target applications for the IPR-SS100C core are:

- Internal interconnect for workstation storage
- Enterprise storage interconnect
- HDD hot-swap environments
- Applications requiring smaller form factor and improved performance SCSI

Features

- Fully compliant to the SAS 3.0Gb/s industry specifications
- AHB-Lite and FPGA specific interfaces for register access
- Supports either SERDES or PHY layer interface
- Fully verified with SAS Verification IP
- Standalone test bench included
- Synchronous design for easy integration
- Synthesizable Verilog design



IPR-SS100C SAS Host Core

SAS Host Core Facts	
Provided with Core	
Documentation	Comprehensive User Documentation
Design File Formats	Post Synthesis EDIF Netlist
Constraints Files	Filename.ucf
Verification	ModelSim verification model
Instantiation Templates	Verilog
Reference Designs & Application Notes	Synthesis or place and route script
Additional Items	Simulation Script , vectors, expected results
Simulation Tool Used	
Cadence Specman Tool	
Support	
The core is delivered and warranted against defects for one year from purchase. Phone and email technical support is included for one year from the purchase date.	

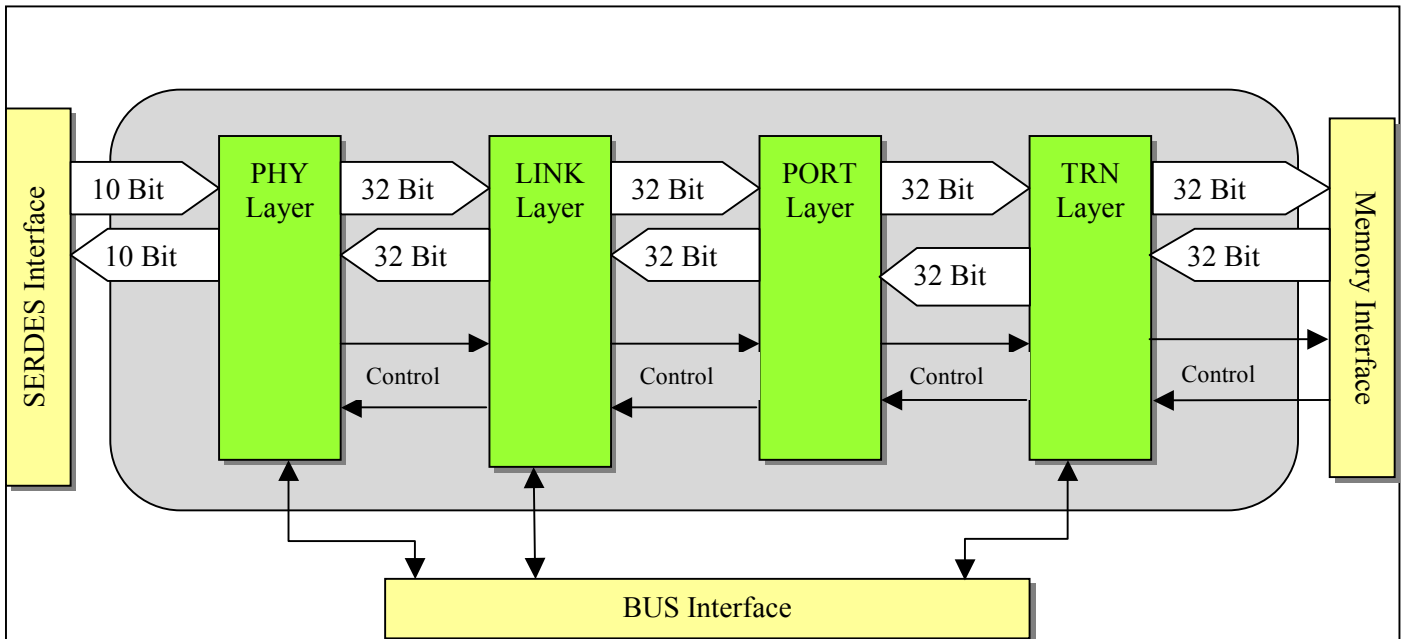


Figure 1 SAS Core Block Diagram

Functional Description

The IPR-SS100C is designed to be connected to a SAS-compliant device application to send and receive Out of Band (OOB) signals, primitives and SAS frames. The SAS host core, as shown in the block diagram, is comprised of four blocks (PHY Layer, LINK Layer, PORT Layer and TRN Layer), and the Bus Interface, SerDes and Memory Interfaces.

Block Descriptions

- Phy Layer and SerDes Interface.

The PHY layer block includes the OOB state machine, 8b/10 encoder and decoder, running disparity checker and logic to check valid dwords and align primitives. The PHY layer also includes a SerDes that can connect to an analog PHY using 10-bit or digital 1-bit interface.

- LINK Layer

The LINK layer block includes the LINK layer state machines, Cyclic Redundancy Check (CRC) generator and scrambler. On the transmit path, when requested by the transport layer, the LINK layer adds onto the SAS frame a Start of Frame (SOF) primitive, a CRC dword and End of Frame (EOF) primitive. The LINK layer state machine sends the frame according to the correct sequence of primitives. The LINK layer also handles any incoming frame on the receive path. Finally, the LINK layer handles all credit transactions, along with connection management.

- PORT (Transport) Layer

The PORT layer block handles port connections and disconnections, using PORT layer state machines.

- TRN (Transport) Layer

The Transport layer of the SAS host core includes multiple transport state machines for both SSP and SMP operation, TX and RX frame control registers to send and receive multiple frames and an interrupt mechanism. The microprocessor interface can be used to control the transport layer block to setup the frames to be transmitted. It is also used to process the received frames.

- Bus Interface

The Bus Interface block provides a pathway for the host system to monitor the SAS host core and provide control instructions. The IntelliProp core has multiple Bus Interfaces to work with the Avalon, PLB, and AHB-Lite buses.

- Data Memory Interface

The Data Memory Interface is designed to give the maximum flexibility to the system designer. It will service from 1 to 16 number of frame memories, depending on the memory and performance needs of the customer.

Support

IntelliProp's SAS Host core is delivered and warranted against defects for one year. Purchase of the SAS core includes phone and email technical support for one year from the purchase date.

Deliverables

The core includes everything required for successful implementation:

- Post-synthesis EDIC netlist or RTL source code
- Self-checking test bench(requires third-party licenses)
- Simulation script, vectors, and expected results
- Synthesis or place and route script
- Comprehensive user documentation

Core Modifications

Modifications are generally not permitted to the SAS host core. Any modifications that are requested must be presented to IntelliProp to determine the feasibility of integrating such changes.

Verification Methods

The SAS Host Core design is used in multiple SAS applications in which it has been tested with multiple drives. Verification done internally at IntelliProp was completed using a constrained random testbench, Specman e and Cadence IUS tools, and a coverage driven methodology.

Recommended Design Experience

Users of the SAS Host Core are expected to have a good working knowledge of SAS Specification 2.04 and application layer knowledge of the SATA protocol.

FPGA Support

IntelliProp's SAS Core is available for integration into devices offered by Altera, Xilinx, and Lattice.

Core Size

IntelliProp's SAS Core size is available on the Products page on the IntelliProp website(<http://www.IntelliProp.com>). If you have questions on our core size, please contact us at info@IntelliProp.com.

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